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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Hisashi Ohtani, et al. Art Unit : 2815
Serial No. : 09/379,702 Examiner : Eugene Lee
Filed : August 24, 1999
Title : METHOD OF FABRICATING SEMICONDUCTOR DEVICES

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REPLY TO ACTION OF FEBRUARY 4, 2004

In reply to the final office action of February 4, 2004, applicant submits the following remarks.

Claims 45-64 are pending in this application, with claims 45-50 being independent.

The claims continue to be rejected as being obvious over Yamazaki in view of Matsumoto. Applicant again asserts that an impermissible hindsight reconstruction of the invention is used to combine Yamazaki and Matsumoto in order to reject the claims. In particular, applicant believes that such impermissible hindsight is used in combining Yamazaki and Matsumoto to obtain the recitation in each of the independent claims that the first insulating film has a side aligned with a side of the crystalline semiconductor island, and that the second insulating film extends beyond an edge of the first insulating film.

Yamazaki shows a gate insulating film 3 that is 0.1 μm thick (see col. 6, line 21, noting a thickness of 1000 Angstroms) and is aligned with a side of a semiconductor crystalline island that is 0.7 μm thick (see col. 6, line 12). A gate electrode that is 0.3 μm thick (see col. 6, lines 22-26) is formed on the gate insulating film.

Matsumoto shows a circuit in which the gate electrode 20 of a NMOS thin transistor 2 of a matrix circuit is separated from a polysilicon thin film 11 by a gate insulating film 14 and an interlayer insulating film 19, while a gate electrode 15 of a NMOS thin film transistor 4 is separated from a polysilicon thin film 12 by only the gate insulating film 14. (See Fig. 1.) While Matsumoto is silent as to the thicknesses of the films 14 and 19, the figures (e.g., Fig. 1) indicate that each of the films 14 and 19 is of roughly the same thickness as the polysilicon films 11 and

12 and the gate electrodes 15 and 20. Thus, using the thicknesses provided by Yamazaki, each of the films 14 and 19 would have a thickness of between is 0.3 μm and 0.7 μm for a combined thickness of between 0.6 μm and 1.4 μm.

The Examiner asserts that a person of ordinary skill in the art would have been motivated to combine Yamazaki and Matsumoto in view of Matsumoto's disclosure that the thin film transistor 2, in which the gate electrode 20 is separated from the polysilicon thin film 11 by the combined thickness of the two films 14 and 19, has better operating characteristics than the thin film transistor 4, in which the gate electrode 15 is separated from the polysilicon thin film 11 by the thickness of the film 14.

Assuming for sake of argument that the statements in Matsumoto would have provided motivation to use a thicker gate insulating film, this could have been done in a number of ways: (1) by replacing Yamazaki's thin gate insulating film with the two thicker films described by Matsumoto; (2) by increasing the thickness of Yamazaki's gate insulating film; (3) by adding a second gate insulating film prior to the etching process illustrated by Yamazaki's Fig. 5C; or (4) by adding a second gate insulating film after the etching process illustrated by Yamazaki's Fig. 5C. The first approach would have resulted in an arrangement in which neither film had a side aligned with the side of the semiconductor island, the second approach would have resulted in an arrangement that included only a single gate insulating film, and the third approach would have resulted in an arrangement in which the second insulating film did not extend beyond an edge of the first insulating film. Only the fourth approach would have resulted in the arrangement of insulating films recited in the claims.

If a person of ordinary skill in the art were to modify Yamazaki in order to obtain the benefits of a thicker gate insulating film as described by Matsumoto, the person would have been much more likely to have taken the first approach, which would have used the two thick films of Matsumoto and provided the same combined film thickness (e.g., between 0.6 μm and 1.4 μm) that produced the beneficial results of Matsumoto, than the fourth approach, which would have employed Yamazaki's thin film and only one of Matsumoto's thicker films for a much reduced combined film thickness (e.g., between 0.4 μm and 0.8 μm). (If the thickness of the films could

be arbitrarily changed, then the person would have been much more likely to use the second approach than the fourth approach in order to avoid the extraneous step of adding a second layer.) If the person were to depart from Matsumoto's use of two films that cover the entire surface of the chip, then the person would have been much more likely to apply the films prior to the etching process illustrated in Fig. 5C (i.e., to take the third approach) than to apply one before and one after (i.e., to take the fourth approach). Thus, absent impermissible hindsight reconstruction of the invention, the alleged benefits of a thicker gate insulating film would not have led the person to combine Yamazaki and Matsumoto in a manner that produces the subject matter claimed.

Enclosed is a $110 check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 6/1/04

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